QuanTalks

IISc Quantum Technologies Initiative (IQTI) Seminar Series

Title: Improving algorithmic performance on quantum computers with optimal control

Abstract: Excitement about the promise of quantum computers is tempered by the reality that the hardware remains exceptionally fragile and error-prone, forming a bottleneck in the development of novel applications. In this talk, I will introduce the concept and experimental implementation of robust quantum control, providing a pathway to maximizing hardware performance in near term systems, and forming a complement to quantum error correction in future systems. We demonstrate ~10X improvements in gate error, resilience against fabrication variance, and resilience against temporal drifts. I will then present the first demonstration of Deep Reinforcement Learning (DRL) to autonomously design a Universal gateset showing superior performance to calibrated default gates. DRL-designed two-qubit cross-resonance gates exhibit ~2.5X improvements relative to standard gates and obviate the need for additional compensating signals designed to mitigate crosstalk. We demonstrate drift-robust two-qubit gate performance at the level of ~99.5% fidelity (near T1 limits) up to 25 days from gate design with no recalibration, while default gates require recalibration every 12-24 hours. We highlight the effectiveness of our techniques by showcasing 25X improvement for 7Q and 100-1000X improvement for 16Q devices in the experimental success probability of quantum algorithms. These experiments reveal a pathway to autonomously designing error-robust quantum logic at scale across complex systems with unknown couplings and Hamiltonian terms.

About the Speaker: Dr. Pranav Mundada is a Senior Quantum Control Engineer at Q-CTRL, where he develops device-cognizant controls for improving hardware performance and accelerating pathways to useful quantum computers. He received the prestigious Porter Ogden Jacobus Fellowship from Princeton University for his Ph.D. thesis on novel qubit design and coupling architectures with superconducting circuits. He completed his undergraduate studies as part of the inaugural UG batch at IISc. Email : pranavm1502@gmail.com

Date & Time
Tuesday, 25th January 2022, 9:00 AM IST

Meeting Link: Click here to join the Webinar