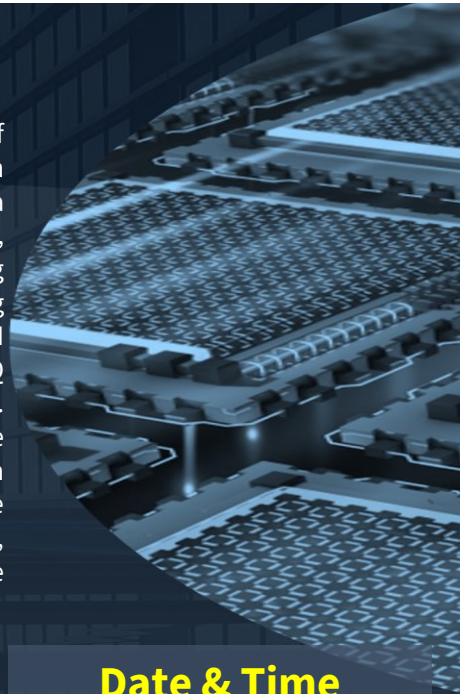
QuanTalks

IISc Quantum Technology Initiative (IQTI) Seminar Series

Title: Super CPU-Microarchitecture Challenges for Building a Superconducting CPU

Abstract: Single Flux Quantum (SFQ) superconducting technology provides significant power and performance benefits in the era of diminishing CMOS scaling. Furthermore, SFQ can help scale quantum computing technologies as SFQ circuits can be integrated with qubit control. Recent advances in design tools and fabrication facilities have brought superconducting CPU (Super CPU) to be a practical CMOS augmentation technology. However, to design a full-fledged Super CPU one must tackle the biggest impediment, namely the availability of dense on-chip memories. Current CPUs use memory extravagantly for all kinds of performance-enhancing (micro)architectural structures, from branch predictors to register files. In this talk, I will first present the basics of superconducting technology and describe why existing memory cell designs in SFQ consume too many Josephson Junctions (JJs) to be viable. Next, I will describe our groups recently proposed High-Capacity Destructive Readout (HC-DRO) cell for doubling the memory density in SFQ technology. HC-DRO design can store up to three fluxon pulses, thereby providing the equivalent of 2-bit storage in a single cell. However, these cells provide only destructive readout capability, namely each value can be read only once. CPU structures rely on the non-destructive readout for achieving the correct functionality. For instance, CPU register file contents are read multiple times between two successive writes; and a branch predictor's history bits are read many times for prediction. Hence, destructive readouts complicate CPU design. To handle these challenges, I will present HiPerRF and SuperBP, a CPU register file, and a branch predictor design, respectively. These designs preserve non-destructive read-out property using a loopback write mechanism, thereby preserving the higher density of HC-DRO cells without compromising the multi-read demands of a register file and branch predictors.



Biography: Prof.Murali Annavaram is a Dean's Chair Professor in the Ming Hsieh Department of Electrical and Computer Engineering, and in the department of Computer Science at the University of Southern California. He currently holds the Smt. Rukmini - Shri. Gopalakrishnachar Visiting Chair Professorship at the Indian Institute of Science, Bengaluru. He is the founding director of the REAL@USC-Meta center which is focused on research and education in AI and learning, and the co-PI of the DISCoVER NSF Expeditions center focused on superconducting technologies. He has been inducted to the hall of fame for three of the prestigious computer architecture conferences ISCA, MICRO, and HPCA. He served as the Technical Program Chair for HPCA 2021 and served as the General Co-Chair for ISCA 2018. Prior to his appointment at USC, he worked at Intel Microprocessor Research Labs from 2001 to 2007. His work at Intel lead to the first 3D microarchitecture paper, and also influenced Intel's TurboBoost technology. In 2020 he was a visiting faculty scientist at Facebook, where he designed checkpoint systems for distributed training. Murali co-authored Parallel Computer Organization and Design, a widely used textbook to teach both the basic and advanced principles of computer architecture. Murali received a Ph.D. degree in Computer Engineering from the University of Michigan, Ann Arbor, in 2001. He is a Fellow of IEEE and a Senior Member of ACM.

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