# QuanTalks

## IISc Quantum Technology Initiative (IQTI) Seminar Series

**Wednesday, 9th August 2023**
**at 4.00 PM (IST)**
**Physics Department**
**Auditorium, IISc**

## Title: Evaluating Fault-Tolerant Schemes For Noisy Hardware

**Abstract:** A large-scale quantum computer is envisioned to leverage the theoretical guarantees of the fault-tolerant accuracy threshold theorem to ensure that long computations be carried out reliably, even in the presence of noise. Quantum Error Correction (QEC) is an integral part of an FT protocol specifying noise-resilient quantum information storage. The conventional approach to fault tolerance using stabilizer codes assumes a simplistic model for errors: probabilistic application of Pauli operations. However, real-world noise is rarely as straightforward as Pauli matrices, e.g., coherent errors that arise from miscalibration. So, a disparity exists between physical noise and oversimplified models for proving the threshold theorems. In this talk, I aim to integrate theoretical and experimental efforts in QEC by addressing the following question. For an n−qubit hardware device, can we efficiently compute a figure of merit that can accurately predict the quality of the logical qubit? Recalling the findings from [1], I will demonstrate that standard error metrics, such as Fidelity, Diamond Distance, and Operator Norms, are not good candidates. Then, I will show some efforts for constructing new measures using machine learning techniques. Through this discussion, I will also point out some nuances in benchmarking QEC methods beyond the Pauli paradigm, which are discussed in [2]. Our outstanding conclusion: Single parameter figures of merit are not good predictors of the efficacy of a QEC scheme. To address our central question, I will discuss a twofold approach detailed in [3]. First, leveraging Randomized Compiling (RC): a method to render complex physics effects on hardware into simple, effective Pauli noise. Second, tricks exploit the structure of concatenated codes to approximate the average logical fidelity of the encoded qubit accurately.

**Related works:**
[1]: Pavithran Iyer and David Poulin. A small quantum computer is needed to optimize fault-tolerant protocols. Quantum Science and Technology, 3(3):030504, 2018. [2]: Pavithran Iyer. Une analyse critique de la correction d'erreurs quantiques pour du bruit realiste. PhD thesis, Universite de Sherbrooke, November 2018.[3]: Pavithran Iyer, Aditya Jain, Stephen D. Bartlett, and Joseph Emerson. Efficient diagnostics for quantum error correction. Phys. Rev. Res., 4:043218, Dec 2022. Other related references: [4]: Pavithran Iyer and David Poulin. chflow: Quantum error correction for realistic noise. https://github.com/paviudes/chflow, 2018. [5]: Aditya Jain, Pavithran Iyer, Stephen D Bartlett, and Joseph Emerson. Improved quantum error correction with randomized compiling. arXiv preprint arXiv:2303.06846, 2023.

## Speaker

**Dr. Pavithran S Iyer**
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## Meeting Link

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**Biography:** Pavithran Iyer (Pavi) is a senior scientist at Xanadu Quantum Technologies, Inc., a quantum computing start-up based in Toronto, Canada. His primary focus is developing quantum error correction techniques for optical hardware employing continuous variable encodings. Pavi has worked on a broad spectrum of problems in fault-tolerant quantum computing over his research career. More details can be found on his webpage: https://sites.google.com/view/piyer/home. Pavi earned his Bachelor's in Physics from Chennai Mathematical Institute in 2008. Subsequently, he completed his Master's in 2014, followed by a Ph.D. in 2018 in Physics from Université de Sherbrooke under the supervision of (late) Prof. David Poulin. Following that, he joined Institute for quantum computing (IQC) as a postdoctoral researcher in the group of Prof. Joseph Emerson until 2021. During this time, Pavi worked as a scientist at Quantum Benchmark, a start-up aimed at error characterization for quantum hardware.