

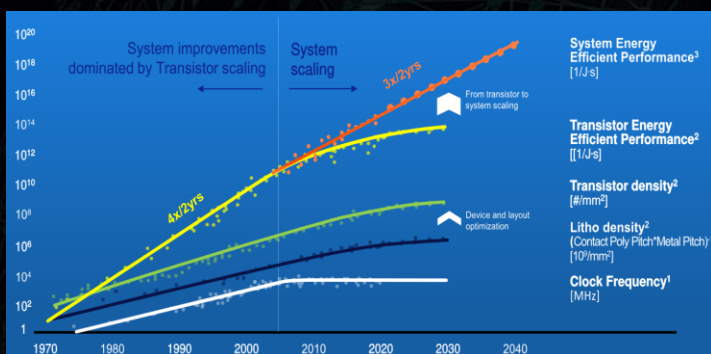


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Physics Auditorium, IISc

The extreme physics at the bleeding edge of Moore's law



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Moore's Law faces challenges as shrinking the transistor approaches its physical limits, compounded by the burgeoning demand for compute power driven by AI applications. While ASML's lithography systems have historically propelled Moore's Law by enabling finer feature patterning, the current landscape demands a paradigm shift towards unconventional methods for scaling Moore's law.

In this presentation, I will highlight the need for creative solutions through the exploration of four distinct scaling techniques to tackle the exponentially growing compute requirements. Through an in-depth analysis of each technique, I will assess their impact on the performance and cost of final integrated circuit chips, unveiling fundamental challenges that lies ahead in realizing the target compute performance. Additionally, I will shed light on various opportunities and solutions that were identified as a direct result of this study. I will highlight few technological solutions that we are actively developing, showcasing the potential they hold for the semiconductor ecosystem.

Syam has been working as a Senior Strategic Researcher at ASML Research Department for almost six years. He has authored eight academic publications and has filed 28 patents spanning a range of fields including semiconductor fabrication (lithography, etching), plasma physics, 2D materials, advanced patterning and metrology.

He devoted the first four years at ASML as a researcher in semiconductor process technology and integration, where he was involved in creating predictive computational models and analyzing experimental data to develop optimal solutions for semiconductor fabrication including patterning and metrology.

For the past three years he has been devoting attention to researching emerging technologies and scaling engines to propel Moore's law. This includes identifying opportunities within and outside ASML's core in market or technology. His job involves scouting for fab equipment opportunities with focus on demonstration of feasibility. One of the spin out as a result of his study focuses on advanced packaging of chiplets which enables faster and energy efficient compute chips. He is also working part time in close liaison with Corporate Market Research where he is assessing the opportunity for ASML within the rapidly growing field of artificial intelligence.

